

Amended Patent Claims

1. Process for forming a housing for electronic modules,
in particular sensors, integrated circuits and
5 optoelectronic components;
comprising the steps of:

- providing a substrate (1) which has one or more
regions comprising semiconductor structures (2) and
comprising connection structures or for forming
10 semiconductor structures (2) and connection structures (3)
and of which at least a first substrate side (1a) is to be
encapsulated,

- providing a vapor-deposition glass source (20),
- arranging the first substrate side (1a) in such a
15 manner with respect to the vapor-deposition glass source
that the first substrate side (1a) can be vapor-coated;

- vapor-coating the first substrate side with a glass
layer (4)

- thinning the substrate (1) on the underside (1b),

- 20 - producing etching pits (6),

- producing line contacts (7) on the underside (1b).

2. The process as claimed in claim 1, wherein the one or
more regions having semiconductor structures (2) are
25 arranged on the first side (1a) of the substrate.

3. The process as claimed in claim 2, wherein the
substrate is provided with a passivation layer (10, 11) on
a second side (1b), which is on the opposite side from the
30 first side (1a).

4. The process as claimed in one of the preceding claims,
the substrate comprising a wafer, wherein the process

comprises the packaging of components which still form part of a wafer.

5. The process as claimed in one of the preceding claims,
5 wherein the substrate (1) is vapor-coated with a glass
layer (4, 10, 11) on two sides (1a, 1b).

6. The process as claimed in one of the preceding claims,
wherein a vapor-deposition glass source (20) which
10 generates at least a binary glass system is provided.

7. The process as claimed in one of the preceding claims,
wherein the vapor-deposition glass source (20) is operated
until the glass layer (4) has a thickness in the range from
15 0.01 to 1000 μm , in particular on the first substrate side.

8. The process as claimed in one of the preceding claims,
wherein as part of the step of providing a vapor-deposition
glass source (20), a reservoir comprising organic
20 constituents is provided, and these organic constituents
are converted into the vapor state through application of a
vacuum or through heating, so that during the vapor-coating
mixed layers comprising inorganic and organic constituents
can be formed on the substrate side.

25 9. The process as claimed in one of the preceding claims,
wherein the glass layer thickness is in the range between
0.1 and 50 μm .

30 10. The process as claimed in one of the preceding claims,
wherein the glass layer thickness is in the range between
50 and 200 μm .

11. The process as claimed in one of the preceding claims,
wherein the vapor-deposition glass of the source (20) is
generated from a glass target (23) by means of electron
5 beam (24).

12. The process as claimed in one of the preceding claims,
wherein the vapor-deposition glass used is a borosilicate
glass containing aluminum oxide and alkali metal oxide
10 fractions.

13. The process as claimed in one of the preceding claims,
wherein the vapor-deposition glass has a coefficient of
thermal expansion which is virtually equal to that of the
15 substrate.

14. The process as claimed in one of the preceding claims,
wherein the glass layer (4) is produced with a thickness
which is required for a hermetic seal, and wherein a layer
20 of plastic (5) is applied above the glass layer (4) in
order to facilitate further processing of the substrate
(1).

15. The process as claimed in one of the preceding claims,
25 wherein a plurality of glass layers are vapor-deposited
onto the substrate (1), it being possible for the glass
layers to consist of various glass compositions.

16. The process as claimed in one of the preceding claims,
30 wherein the further processing of the substrate (1)
involves the removal of material from a second substrate
side (1b), which is on the opposite side from the first
substrate side (1a).

17. The process as claimed in one of the preceding claims,
wherein the substrate (1) includes a wafer having a
plurality of semiconductor structures (2) and connection
5 structures (3), with the second substrate side (1b), which
is on the opposite side from the first substrate side (1a),
being thinned, pits (6) being etched on the second
substrate side (1b) in the region of the connection
structures to be produced, the regions for forming the
10 semiconductor structures (2) being lithographed using
plastic layers,
line contacts (7) being produced on the second substrate
side (1b) in the regions having connection structures (3),
the plastic being removed from the second substrate side
15 (1b), a ball grid array (8) being applied at the line
contacts (7), and
the wafer being divided up so as to form a plurality of
electronic modules which each have first, encapsulated
sides (1a).

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18. The process as claimed in claim 17, wherein the second
substrate side (1b) is provided with a plastic covering
(10) while leaving clear the ball grid regions (8).

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19. The process as claimed in claim 17 or 18,
wherein after the plastic has been removed from the second
substrate side (1b) the whole of the second substrate side
is vapor-coated with a glass layer (11), and wherein the
line contacts (7) are uncovered by local elimination of the
30 glass layer (11), after which the steps of applying the
ball grid array (8) and of dividing up the wafer are
carried out in order to obtain electronic modules which are
encapsulated on both sides.

20. The process as claimed in claim 19, wherein the entire second substrate side is vapor-coated with a glass layer (11) with a thickness in the range from 1 to 50 μm , and

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21. The process as claimed in one of claims 17 to 20, wherein the etching pits (6) which lead to the connection structures (3) are filled with conductive material (12), after which, with or without removal of the plastic (10) from the second substrate side (1b) and with or without a glass layer (11) on the second substrate side (1b), and leaving clear the line contacts (7), the ball grid array (8) is applied at the line contacts (7) and/or at the filling material.

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22. The process as claimed in one of the preceding claims, wherein the vapor-coating of the first substrate side (1a) with a glass layer (4) comprises plasma ion assisted deposition (PIAD).

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23. An electronic module, in particular as a sensor or as an integrated circuit or as an optoelectronic component, producible by the process as claimed in one of the preceding claims.

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24. The electronic module as claimed in claim 23, which on a first side (1a) has one or more regions with semiconductor structures (2), and connection structures (3), wherein the substrate is coated with a vapor-deposited glass layer (4) on at least one side.

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25. The electronic module as claimed in claim 24, wherein a plastic layer (5) which reinforces the module is applied to the glass layer (4).

5 26. The electronic module as claimed in one of claims 24 or 25, wherein the substrate is thinned.

10 27. The electronic module as claimed in one of claims 24 to 26, wherein the substrate is provided with a passivation layer (10, 11) on a second side (1b), which is on the opposite side from a first side (1a) having semiconductor structures and connection structures.

15 28. The electronic module as claimed in one of claims 24 to 27, wherein the glass layer (4) comprises a mixed layer of inorganic and organic constituents.

20 29. The electronic module as claimed in one of claims 24 to 28, which includes a multilayer glass layer (4).

30. The electronic module as claimed in claim 29, wherein the individual layers of the glass layer have different compositions.

25 31. The electronic module as claimed in one of claims 24 to 30, wherein the substrate (1), on a second side (1b), has line contacts that are connected to connection structures on the first side (1a).

30 32. The electronic module as claimed in claim 31, which includes a ball grid array (8) at the line contacts.